

## 4A, 650V N-CHANNEL POWER MOSFET

### DESCRIPTION

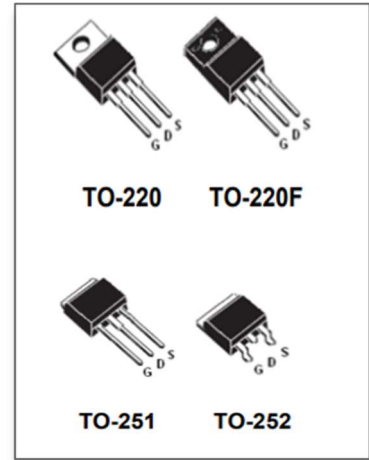
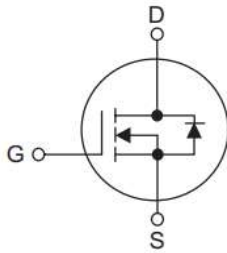
The **4N65** is a high voltage power MOSFET designed to have better characteristics, such as fast switching time, low gate charge, low on-state resistance and have a high rugged avalanche characteristic. This power MOSFET is usually used in high speed switching applications including power supplies, PWM motor controls, high efficient DC to DC converters and bridge circuits.

### FEATURES

- \* $R_{DS(ON)} < 2.5\Omega @ V_{GS} = 10V$
- \*Fast Switching Capability
- \*Avalanche Energy Specified
- \*Improved  $dv/dt$  Capability, High Ruggedness

### SYMBOL

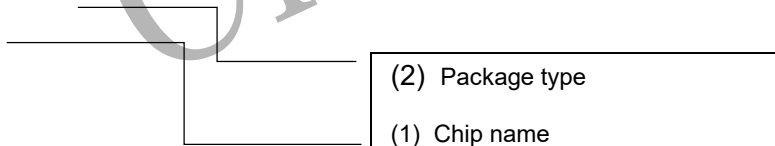
1. Gate
2. Drain
3. Source



### Package Description

Product Model	Package Type	Mark Name	Identification Code	Package
CMN4N65P	TO-220	CMN4N65	P	Tube
CMN4N65F	TO-220F	CMN4N65	F	Tube
CMN4N65U	TO-251	CMN4N65	U	Tube
CMN4N65D	TO-252	CMN4N65	D	Tape Reel

CMN4N65P



(1) CMN4N65: 650V 4A (2) F:TO-220F P:TO-220 D:TO-252 U:TO-251

**ABSOLUTE MAXIMUM RATINGS** (TC = 25°C, unless otherwise specified)

PARAMETER		SYMBOL	RATINGS	UNIT
Drain-Source Voltage		V <sub>DSS</sub>	650	V
Gate-Source Voltage		V <sub>GSS</sub>	±30	V
Avalanche Current (Note 2)		I <sub>AR</sub>	4.4	A
Drain Current	Continuous(Tc=25°C)	I <sub>D</sub>	4.0	A
	Continuous(Tc=100°C)		2.5	A
	Pulsed (Note 2)	I <sub>DM</sub>	16	A
Avalanche Energy	Single Pulsed (Note 3)	E <sub>AS</sub>	260	mJ
	Repetitive (Note 2)	E <sub>AR</sub>	10.6	mJ
Peak Diode Recovery dv/dt (Note 4)		dv/dt	4.5	V/ns
Power Dissipation	Tc=25°C	TO-220	106	W
		TO-220F	35	W
		TO-252/TO-251	50	W
Junction Temperature		T <sub>J</sub>	+150	°C
Operating Temperature		T <sub>OPR</sub>	-55~+150	°C
Storage Temperature		T <sub>STG</sub>	-55~+150	°C

Note:

- Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.
- Repetitive Rating: Pulse width limited by maximum junction temperature.
- L = 30mH, I<sub>AS</sub> = 4A, V<sub>DD</sub> = 50V, R<sub>G</sub> = 25 Ω, Starting T<sub>J</sub> = 25°C
- ISD ≤ 4.4A, di/dt ≤ 200A/μs, V<sub>DD</sub> ≤ BVDSS, Starting T<sub>J</sub> = 25°C

**THERMAL CHARACTERISTICS**

Symbol	Parameter	PACKAGE	RATINGS	Units
R <sub>θJC</sub>	Junction-to-Case	TO-220	1.18	°C/W
		TO-220F	3.5	°C/W
		TO-252-TO-251	2.5	°C/W
R <sub>θJA</sub>	Junction-to-Ambient	TO-220F/TO-220	62.5	°C/W
		TO-252-TO-251	110	°C/W

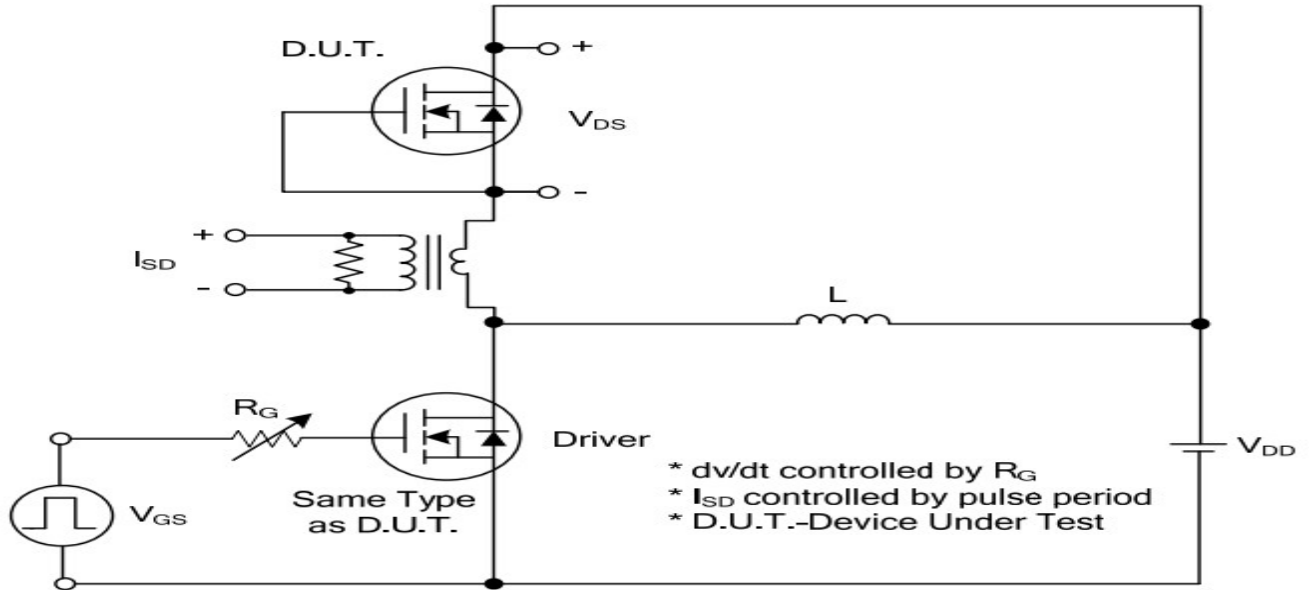
**ELECTRICAL CHARACTERISTICS** ( $T_C = 25^\circ\text{C}$ , unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>OFF CHARACTERISTICS</b>						
Drain-Source Breakdown Voltage	$BV_{DSS}$	$V_{GS} = 0\text{ V}, I_D = 250\mu\text{A}$	650		900	V
Drain-Source Leakage Current	$I_{DSS}$	$V_{DS} = 650\text{ V}, V_{GS} = 0\text{ V}$			120	nA
Gate-Source Leakage Current	Forward	$V_{GS} = 30\text{ V}, V_{DS} = 0\text{ V}$			100	nA
	Reverse	$V_{GS} = -30\text{ V}, V_{DS} = 0\text{ V}$			-100	nA
<b>ON CHARACTERISTICS</b>						
Gate Threshold Voltage	$V_{GS(TH)}$	$V_{DS} = V_{GS}, I_D = 250\mu\text{A}$	2.3		3.8	V
Static Drain-Source On-State Resistance	$R_{DS(ON)}$	$V_{GS} = 10\text{ V}, I_D = 2\text{ A}$	1.5		2.6	$\Omega$
<b>DYNAMIC CHARACTERISTICS</b>						
Input Capacitance	$C_{ISS}$	$V_{DS} = 25\text{ V}, V_{GS} = 0\text{ V}, f = 1\text{ MHz}$	520	524	529	pF
Output Capacitance	$C_{OSS}$		62			pF
Reverse Transfer Capacitance	$C_{RSS}$		10			pF
<b>SWITCHING CHARACTERISTICS</b>						
Total Gate Charge	$Q_G$	$V_{DS} = 520\text{ V}, I_D = 4.0\text{ A}, V_{GS} = 10\text{ V}$ (Note 1, 2)		100	120	nC
Gate-Source Charge	$Q_{GS}$		17	19	nC	
Gate-Drain Charge	$Q_{GD}$		20	26	nC	
Turn-On Delay Time	$t_{D(ON)}$	$V_{DS} = 325\text{ V}, I_D = 4.0\text{ A}, R_G = 25\Omega$ (Note 1, 2)		45	85	ns
Turn-On Rise Time	$t_r$		100	140	ns	
Turn-Off Delay Time	$t_{D(OFF)}$		200	240	ns	
Turn-Off Fall Time	$t_f$		130	150	ns	
<b>SOURCE- DRAIN DIODE RATINGS AND CHARACTERISTICS</b>						
Maximum Continuous Drain-Source Diode Forward Current	$I_S$				4.4	A
Maximum Pulsed Drain-Source Diode Forward Current	$I_{SM}$				17.6	A
Drain-Source Diode Forward Voltage	$V_{SD}$	$V_{GS} = 0\text{ V}, I_S = 4\text{ A}$	0.7		1.4	V
Reverse Recovery Time	$t_{rr}$	$V_{GS} = 0\text{ V}, I_S = 4.4\text{ A}, dI_F/dt = 100\text{ A}/\mu\text{s}$ (Note 1)		250		ns
Reverse Recovery Charge	$Q_{rr}$			1.5		$\mu\text{C}$

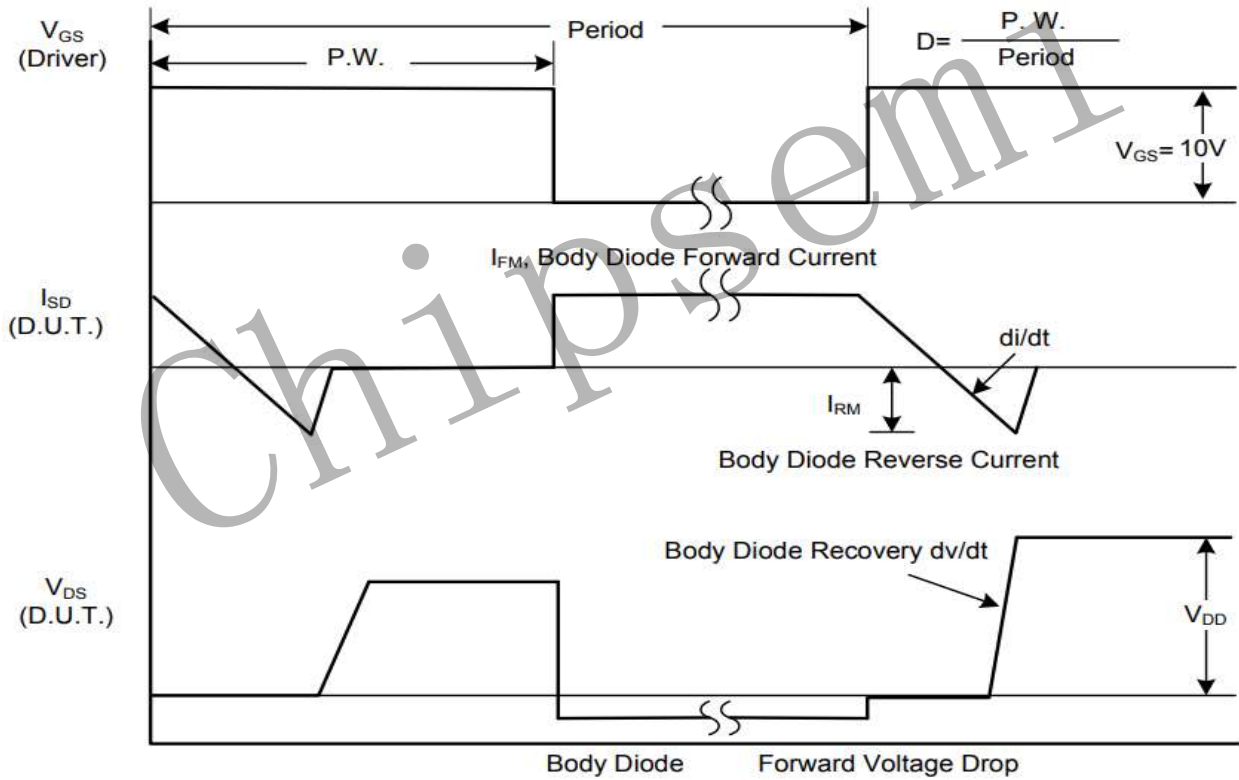
Note:

1. Pulse Test: Pulse width $\leq 300\mu\text{s}$ , Duty cycle $\leq 2\%$ .
2. Essentially independent of operating temperature

TEST CIRCUITS AND WAVEFORMS

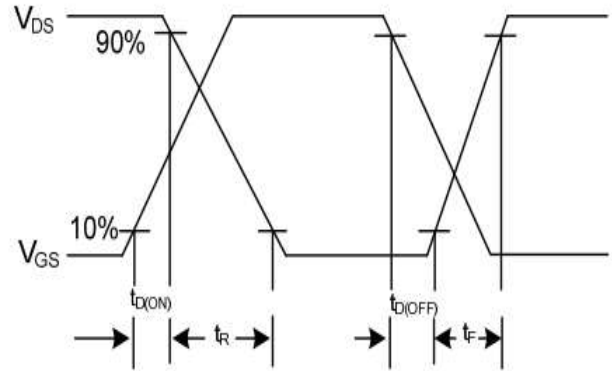
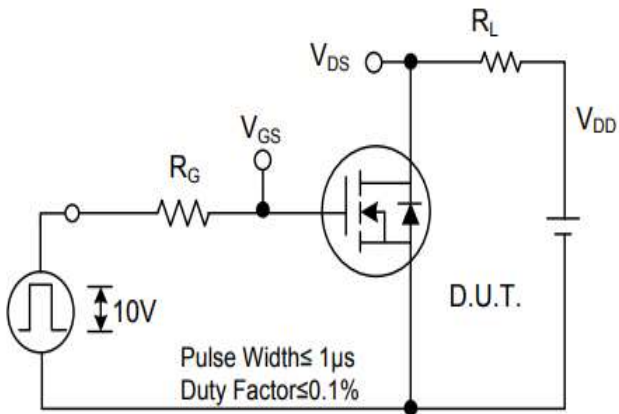


Peak Diode Recovery dv/dt Test Circuit



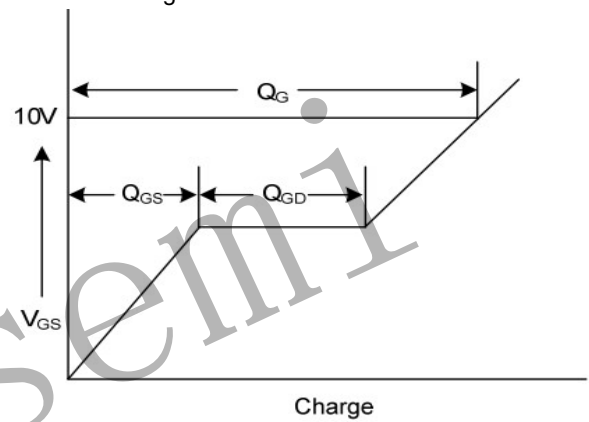
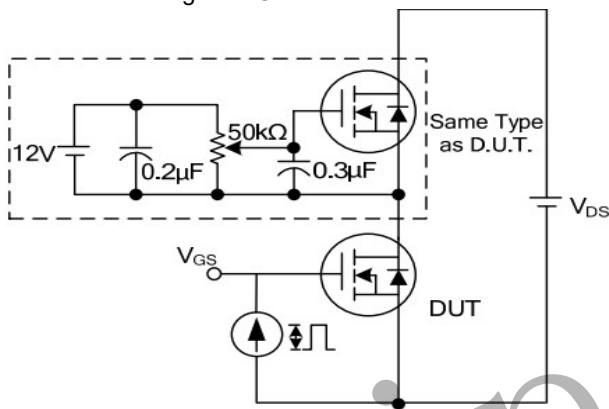
Peak Diode Recovery dv/dt Waveforms

TEST CIRCUITS AND WAVEFORMS(Cont.)



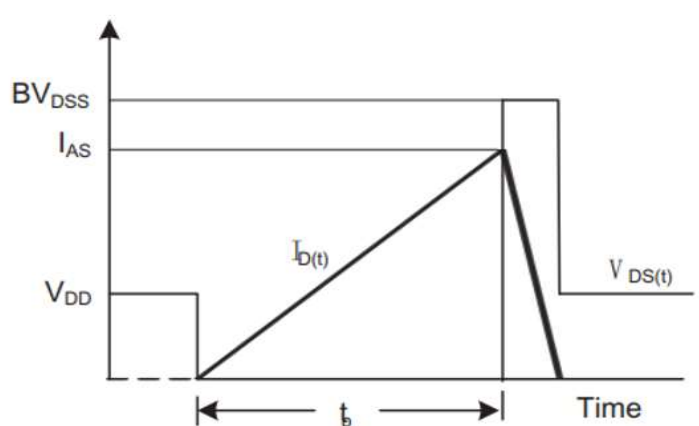
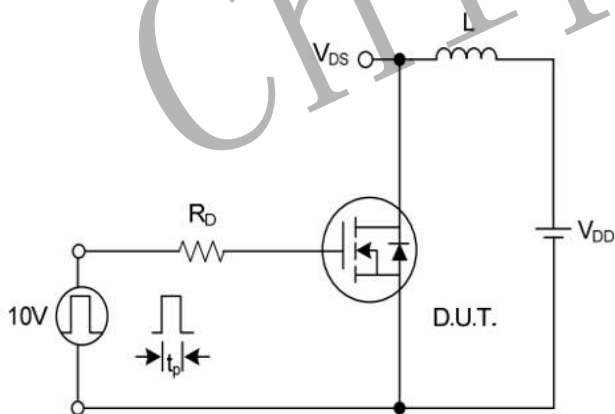
Switching Test Circuit

Switching Waveforms



Gate Charge Test Circuit

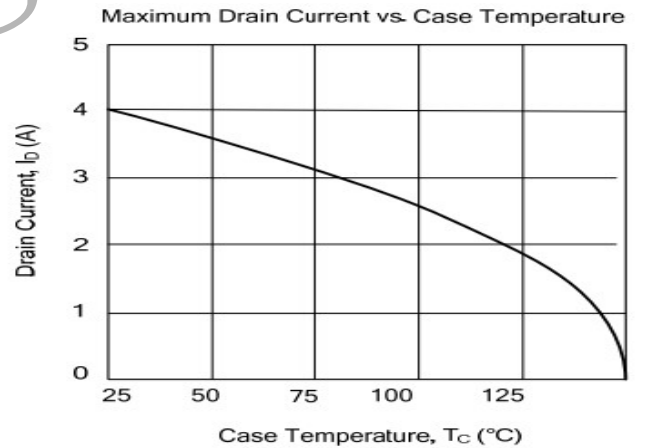
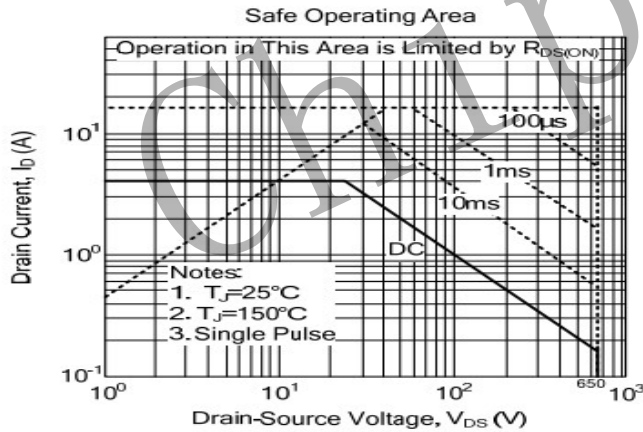
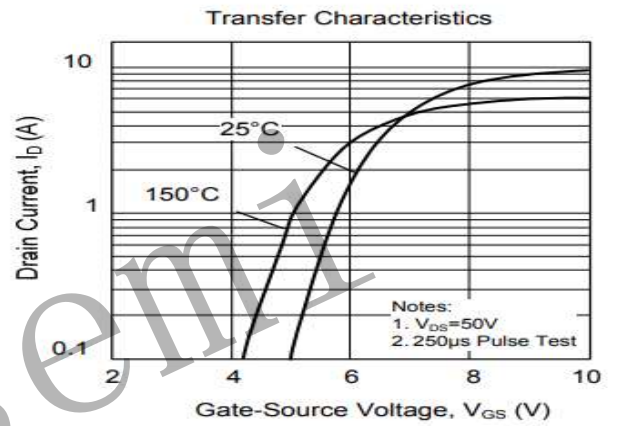
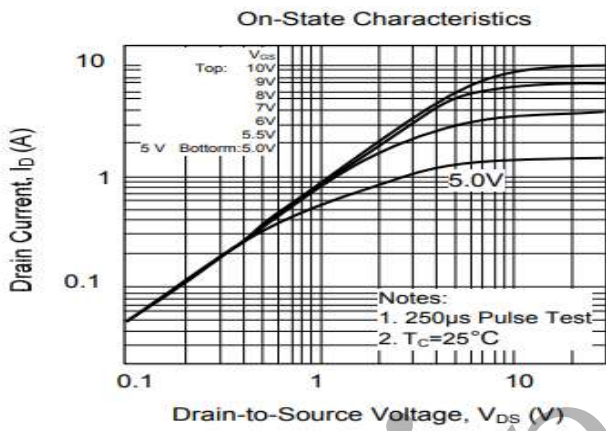
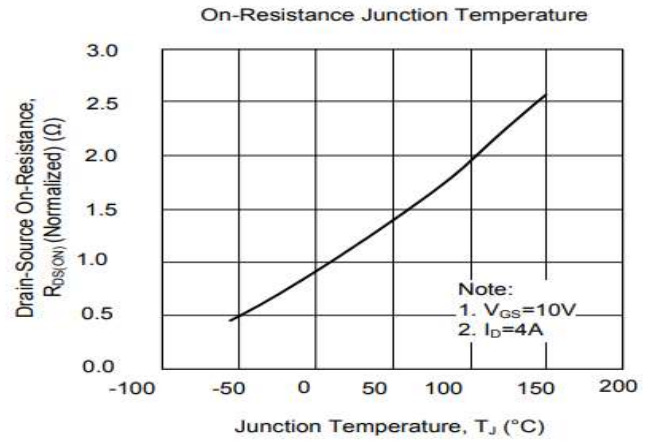
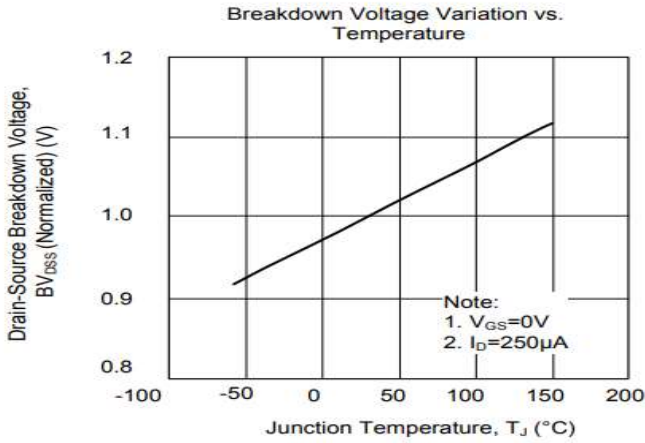
Gate Charge Waveform



Unclamped Inductive Switching Test Circuit

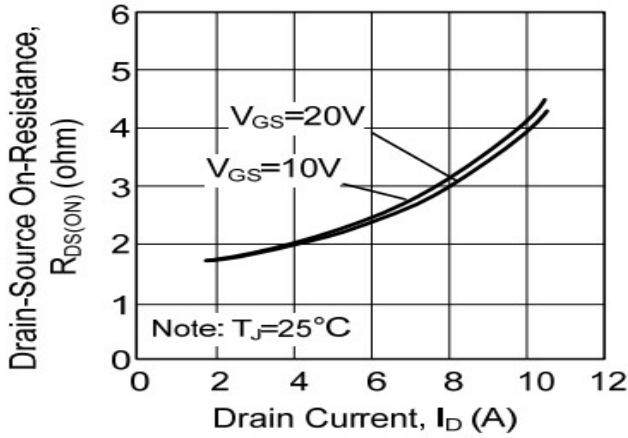
Unclamped Inductive Switching Waveforms

YPICAL CHARACTERISTICS

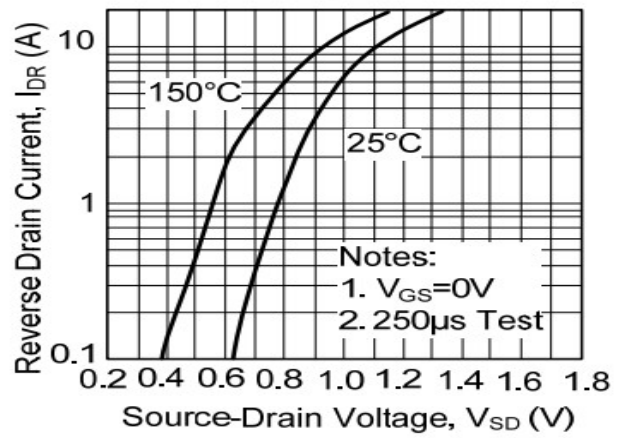


TYPICAL CHARACTERISTICS (Cont.)

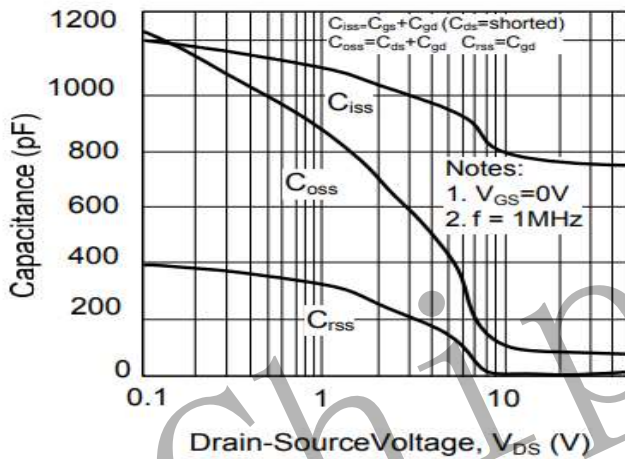
On-Resistance Variation vs. Drain Current and Gate Voltage



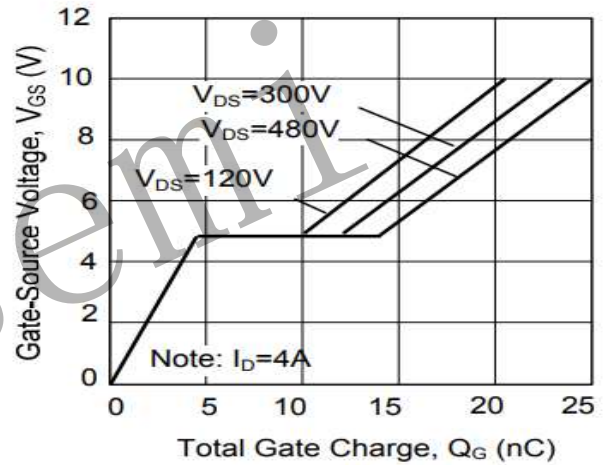
On State Current vs. Allowable Case Temperature



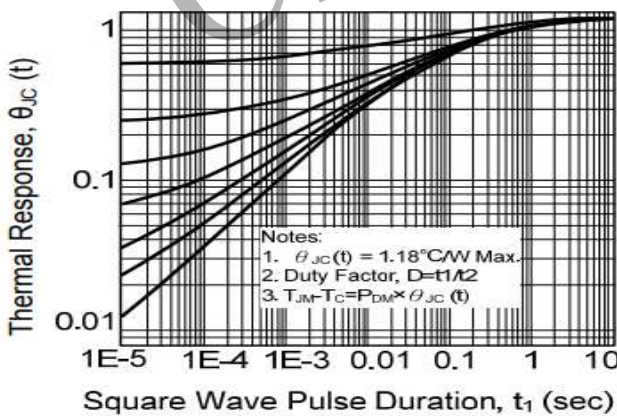
Capacitance Characteristics (Non-Repetitive)



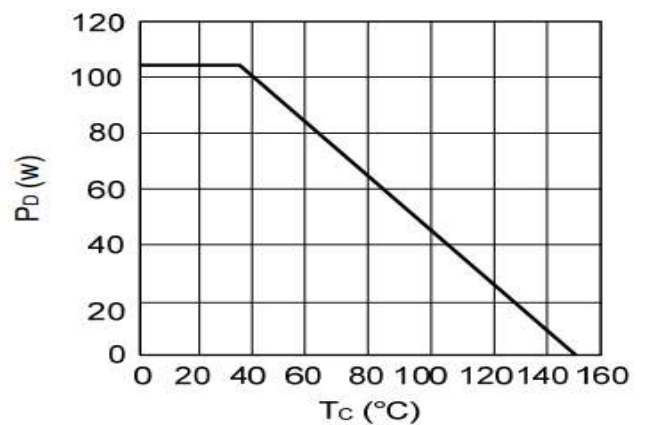
Gate Charge Characteristics



Transient Thermal Response Curve



Power Dissipation



## Attentions

- Exceeding the maximum ratings of the device in performance may cause damage to the device, even the permanent failure, which may affect the dependability of the machine. Please do not exceed the absolute maximum ratings of the device when circuit designing.
- When installing the heat sink, please pay attention to the torsional moment and the smoothness of the heat sink.
- MOSFET is the device which is sensitive to the static electricity, it is necessary to protect the device from being damaged by the static electricity when using it.
- Chipsemi reserves the right to make changes in this specification sheet and is subject to change without prior notice.

## Appendix

Revision history:

Date	REV.	Description	Page
2023.3	1.0	Original	8

Chipsemi